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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,017	09/30/2003	Myoung-Kee Baek	8734.240.00 US	2379

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EXAMINER	
TALBOT, BRIAN K	
ART UNIT	PAPER NUMBER
1715	
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11/08/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,017	BAEK ET AL.	
	Examiner	Art Unit	
	Brian K. Talbot	1715	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10,12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10,12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The amendment filed 9/20/10 has been considered and entered. Claims 4,11,13 have been canceled. Claims 1-3,5-10,12 and 14-19 remain in the application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

4. Claims 1-3,6-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) both (a) or (b) in combination with Kikuchi et al. (4,704,002).

Hattori et al. (5,403,616) teaches a method of forming patterned transparent conductive film. The patterning process comprises forming a masking pattern (2) on a substrate (10),

applying the coating layer (3), heating the coating layer and the mask to set the coating layer and remove the mask to form the patterned layer (abstract, Figs. 1a-1e, 2a-2e and col. 2, line 60 – col. 3, line 65). Hattori et al. (5,403,616) teaches the process utilized for LCD devices (col. 1, lines 9-25). The glass substrate can have a coating of silica thereon prior to the application of the patterned coating layer (examples). The coating layer can be applied by spin coating, dip coating or roll coating (col. 4, lines 41-64). Hattori et al. (5,403,616) teaches physically removing the masking pattern by ultrasonic cleaning or gas jet of air (col. 4, lines 28-40).

Hattori et al. (5,403,616) fails to teach a master being separately formed and separable from the substrate. In addition, the use of a doctor blade to planarize the resist coating for claims 10-13.

JP 08-031,830 teaches a solder bump forming process whereby a mask is set with a distance above the substrate and solder is filled in the mask. The solder can be placed on the substrate by die punching (Figs. 1A-1D) or by being close enough to the substrate (Figs. 4A-4D).

Therefore, it would have been obvious for one skilled in the art at the time the invention was made to have modified Hattori et al. (5,403,616) process by substituting a "displaced mask" as evidenced by JP 08-031,830 for the mask of Hattori et al. (5,403,616) with the expectation of achieving similar success.

(a) Hattori et al. (5,403,616) in combination with JP 08-031,830 fail to teach a distance between the master and substrate being a few micrometers.

While this may be the case, it is the Examiner's position that the distance between the mask and the substrate would be a matter of design choice of one practicing in the art depending upon the desired end product. It is would be within the skill of one practicing in the art to

separate the mask from the substrate at a "distance" equal to or slightly greater than the "height" of the paste being applied to assure placement upon the substrate. These parameters are "result effective variables" which are deemed as an unpatentable distinction over the art absent a showing of unexpected results.

(b) Hattori et al. (5,403,616) in combination with JP 08-031,830 fail to teach a distance between the master and substrate being a few micrometers.

Yamuni et al. (6,730,358) teaches a method for depositing conductive paste using stencil whereby a mask having a thickness of 0.001-0.008 microns being displaced from the substrate and the pins are about greater than 40% of the length of the aperture to from the coating (col. 4, lines 32-40 and col. 6, lines 50-63). With this in mind the distance between the mask and the substrate must be equal to or less then the thickness of the mask and therefore meets the claimed invention. This is the same argument presented by applicant in the response filed 1/28/09, i.e. there is a correspondence between thickness of mask and distance between mask and substrate.

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified Hattori et al. (5,403,616) in combination with JP 08-031,830 process to have a distance between the master and substrate being a few micrometers as evidenced by Yamuni et al. (6,730,358) with the expectation of achieving similar success.

Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) both fail to teach a stepped etching layer.

Features detailed above concerning Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) are incorporated here.

Kikuchi et al. (4,704,002) depicts and teaches a display panel having stepped portions whereby photomasks are utilized to form the layers (abstract, col. 2, line 40 – col. 3, line 25 and Figs. 10b-17b).

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) process to incorporate a stepped etching layer as evidenced by Kikuchi et al. (4,704,002) with the expectation of achieving similar success, i.e. a patterned layer for LCD and TFT manufacture.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) either (a) or (b) further in combination with Kikuchi et al. (4,704,002) and still further in combination with Applicant's admitted state of the art (specification pg. 2-5 and Figs. 1-2).

Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) in combination with Kikuchi et al. (4,704,002) fail to teach and etching layer being metal.

Applicant's admitted state of the art (specification pg. 2-5 and Figs. 1-2) teaches that gate electrodes, drain electrodes and pixel electrodes are formed on a glass substrate for LCD manufacture.

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified over Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Yamuni et al. (6,730,358) in combination with Kikuchi et al. (4,704,002) process by including a metal electrode layer to be etched as evidenced by Applicant's admitted state of the art (specification pg. 2-5 and Figs. 1-2) with the expectation of achieving similar success, i.e. a patterned layer.

5. Claims 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (5,403,616) in combination with JP 08-031,830 (a) alone or (b) further in combination with Kikuchi et al. (4,704,002) further in combination with Peek (4,301,191).

Hattori et al. (5,403,616) in combination with JP 08-031, 830 (a) alone or (b) in combination with Kikuchi et al. (4,704,002) fail to teach the distance between the master and the substrate being from 1-9 microns.

Peek (4,301,191) teaches a method of forming conductors by applying the conductive material through a mask located a small distance from the substrate (abstract). Peek (4,301,191) teaches a distance between the mask and the substrate to be 2 microns (col. 4, lines 45-50 and col. 6, lines 35-45).

Therefore it would have been obvious at the time the invention was made to have modified Hattori et al. (5,403,616) in combination with JP 08-031, 830 (a) alone or (b) in

combination with Kikuchi et al. (4,704,002) process to position the mask at a distance of 2 microns as evidenced by Peek (4,301,191) with the expectation of achieving similar success, i.e. a pattern coating.

Response to Amendment

6. Applicant's arguments with respect to claims 1-3,5-10,12 and 14-19 have been considered but are not found persuasive.

Applicant argued that the prior art fails to teach etching the etching layer using the resist pattern as a mask to form a stepped portion of the etching layer.

The Examiner disagrees. Kikuchi et al. (4,704,002) depicts and teaches a display panel having stepped portions whereby photomasks are utilized to form the layers (abstract, col. 2, line 40 – col. 3, line 25 and Figs. 10b-17b). The photomask is the resist layer in the claimed invention and the silica coating layer on the glass substrate of Hattori et al. (5,403,616).

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian K Talbot/
Primary Examiner, Art Unit 1715

BKT